BE | VII | CBGS | (New) | DC | Electronics | | 17/05/16

QP Code : 31293

Time: 3 Hours. Sub:- DC Technology

Max. Marks: 80

N.B.

1) Question No. 1 is compulsory
2) Solve any three questions from the remaining questions
3) Assume suitable data if necessary

1. Solve any four of the following (20)
   (a) Explain Interstitial and substitutional diffusion process.
   (b) Explain Electronics package reliability.
   (c) Explain the concept of clean rooms.
   (d) Explain Nuclear and electronic stopping mechanisms in Ion implantation with neat diagrams
   (e) Give the steps in a standard RCA cycle during wafer cleaning

2.
   (a) What is Ion Implantation? Explain the process with a neat diagram. (10)
   (b) Describe optical lithography with the help of a neat diagram. (10)

3.
   (a) Explain the fabrication process step along with vertical cross-sectional views for CMOS Inverter using twin tub process. (10)
   (b) With neat diagram explain the Float Zone technique of crystal growth. (10)

4.
   (a) What is the significance of Design rules? Draw layout for the CMOS inverter using lambda (λ) based design rules. (10)
   (b) Discuss Etching methods for photoresists removal. (10)

5.
   (a) Explain SOI fabrication using bonded SOI and smart cut method. (05)
   (b) State advantages of BICMOS over CMOS (05)
   (c) Describe with the help of a neat diagram Hayness-Schokley experiment for measurement of Drift Mobility of n-type semiconductor. (10)

6. Write short notes on any four of the following (20)
   (a) MODFET and optoelectronics devices
   (b) Nanowire transistor
   (c) Molecular Beam epitaxy
   (d) Second order effects in bipolar transistor
   (e) VLSI Technology Trends affecting Testing